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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VO, THANH DUC	
ART UNIT	**PAPER NUMBER**
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,149	MACLAREN ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on April 3, 2007. Claims 1-19 are presented for examination. Claims 1-19 are pending. All objections and rejections that are not repeated below have been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-3, 6, 8-11, 13, 14, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Piccirillo et al. (hereinafter Piccirillo) of U.S. Publication No. 2002/0053010.

As per claims 1, 10, 14, and 17 Piccirillo substantially discloses a computer system, comprising:

a processor running an operating system (see abstract, computer system, wherein an operating system and processor are an inherent features); and

a memory subsystem (Fig. 1, items 25) coupled to said processor (Fig. 1, item 12), said memory subsystem 25 comprising a memory controller (Fig. 1, item 20) and a plurality of memory modules (Fig. 6, items 25a-e) coupled to said memory controller;

wherein a newly inserted memory module is present in the computer system but isolated wherein transactions that target said newly inserted memory module can complete without loss of data and without accessing said newly inserted memory module, and while isolated, said newly inserted memory module is tested. See paragraph [0088], lines 21-27, wherein the user inserts a new memory module into the system but it is not operating with other memory module in the redundant mode until the memory is verified that it has not fault. Further clarification can be found on the paragraph [0089].

As per claim 2, Piccirillo discloses a computer system, wherein the memory subsystem comprises redundancy and data is not lost due to the redundancy of the memory subsystem. See paragraph [0088] lines 5-7.

As per claims 3, 11, and 15 Piccirillo disclosed a computer system, wherein the memory subsystem comprises a RAID subsystem and read and write transactions can be completed that target said isolated memory module without loss of data using data from other memory modules. See paragraph [0052] lines 1-5.

As per claims 6 and 13, Piccirillo discloses a computer system, wherein the memory subsystem comprises a mirror configuration in RAID level 1. See page 2 paragraph 0024.

As per claim 8, Piccirillo disclosed a computer system wherein, when isolated, an isolated memory module is isolated upon insertion into said system. See paragraph 0088, lines 21-23.

As per claim 9, Piccirillo discloses a computer system wherein the plurality of memory modules comprises hot plug modules. See paragraph 0088, lines 1-3.

As per claim 18, Piccirillo discloses a method wherein upon completing the testing, the isolation is terminated and permitting the access to the hot plug memory. See paragraph 0088, lines 26-27, the memory is back to operating in redundant mode after rebuild and verification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 5, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Piccirillo et al. (hereinafter Piccirillo) of U.S. Publication 2002/0053010 in view of McKenzie of U.S. Patent 6,453,398.

As per claims 4, 5, and 12, Piccirillo did not explicitly disclose a memory module that may be isolated includes its own test logic.

McKenzie disclosed a memory includes its own test logic. See col. 2, lines 30-35.

Piccirillo and McKenzie are from the same field of endeavor, memory testing and redundancy.

At the time of the Applicant's invention, it would have been obvious to one having an ordinary skill in the art to modify the system of Piccirillo to include its own test logic as taught by McKenzie.

The motivation of doing so is to enable the each of the memory module to test itself while the memory system can function normally without interruption or affecting the access time of the other memory modules as taught by McKenzie in col. 2, lines 32-36.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Piccirillo with the method of McKenzie to arrive at the invention claimed in claims 4, 5 and 12.

4. Claims 7, 16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Piccirillo et al. (hereinafter Piccirillo) of U.S. Publication 2002/0053010 and further in view of Nakamura et al. (hereinafter Nakamura) of U.S. Patent 5,706,407.

As per claims 7, 16 and 19, Piccirillo failed to teach an SMI handler that runs code to test a memory module when isolated and said computer system further includes a memory map having a plurality of addresses, a first range of addresses corresponding to said isolated memory module and a second range of addresses that is mapped to said first range to permit said SMI handler access to said isolated memory module to run its code.

Nakamura taught an SMI handler (Fig. 4, item 14, and page col. 13, line 65 – 14, line 6) that runs code.

Nakamura further taught a memory system includes a memory map having a plurality of address (Fig. 4), a first range of address (main memory area 13, and col. 14, lines 11-15) is reserved for system operation, and a second range of address is reserved for SMI handler (col. 14, lines 45-49, BIOS).

Piccirillo and Nakamura are from the same field of endeavor, memory management.

At the time of the Applicant's invention, it would have been obvious to one having an ordinary skill in the art to realize that the it is advantageous to combine the method of Piccirillo with the method of Nakamura.

The motivation of doing is so is to enable the system of Piccirillo to virtually and physically assigned address regions in the CPU and memory so that the system of Piccirillo could efficiently carry out the operation from an OS to test the memory by assigning the SMI handler in the BIOS and storing information of an isolated memory module into the main memory area which result a reduced the processing time since it

is operating at the CPU and system memory level as taught by Nakumura at col. 13 lines 65 – col. 14, lines 6, and col. 14, lines 31-40.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Piccirillo to combine with the system of Nakamura in order to arrive at the invention claimed in claims 7 and 16.

Response to Arguments

5. Applicant's arguments filed April 3, 2007 have been fully considered but they are not persuasive.

In the Remarks/Argument filed on April 3, 2007 Applicant stated that Piccirillo does not teach the following as being claimed in claim 1 of the current invention:

a. Completing transactions to an isolated memory module while the isolated memory module is being tested.

b. Transactions are permitted to occur to a newly replaced DIMM while the DIMM is being verified.

With respect to (a) and (b), the limitation in claim 1 is actually read as "wherein transactions **that target said isolated memory** module can be completed without loss of data and without accessing said isolated memory, and while isolated, said memory module is tested." (Emphasis added)

As the language of claim 1 is written as quoted above, the transactions are rather targeting the isolated memory; therefore, Piccirillo substantially discloses in paragraph 0088, lines 5-10 such limitation. On paragraph 0088, lines 5-10, Piccirillo discloses a

fault-tolerant memory system to allow the user to remove and replace a failed memory without significantly impacting normal system operation and without requiring the system to be powered down. In doing so, while the failed memory is not operational but any transactions that supposedly target to the failed memory can be completed since Piccirillo's system is a fault-tolerant memory configuration.

With respect to (b), there's nowhere in claim 1 that states, "transactions are permitted to **occur** to a newly replaced DIMM (memory) while the DIMM is being verified". As noted above, claim 1 only claim that transactions that target the DIMM (memory); therefore, there is no transactions that are specifically occurred to a newly replaced memory.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh D. Vo
Patent Examiner
AU 2189
5/15/2007

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